深圳市阿美林电子科技有限公司

Shenzhen Amelin Electronic Technology Co. ,Ltd

SPECIFICATION

产 品 规 格 书

Project No. 项目编号	AML080C01ABE00C-00
Customer 客户名称	
Module No. 客户型号	
Product type 产品内容	Standard LCD Module 800x 3RGB x1280 Dots 8.0”TFTLCD

Signature by customer:

客户确认签章：

PREPARED BY	CHECKED BY	APPROVED BY

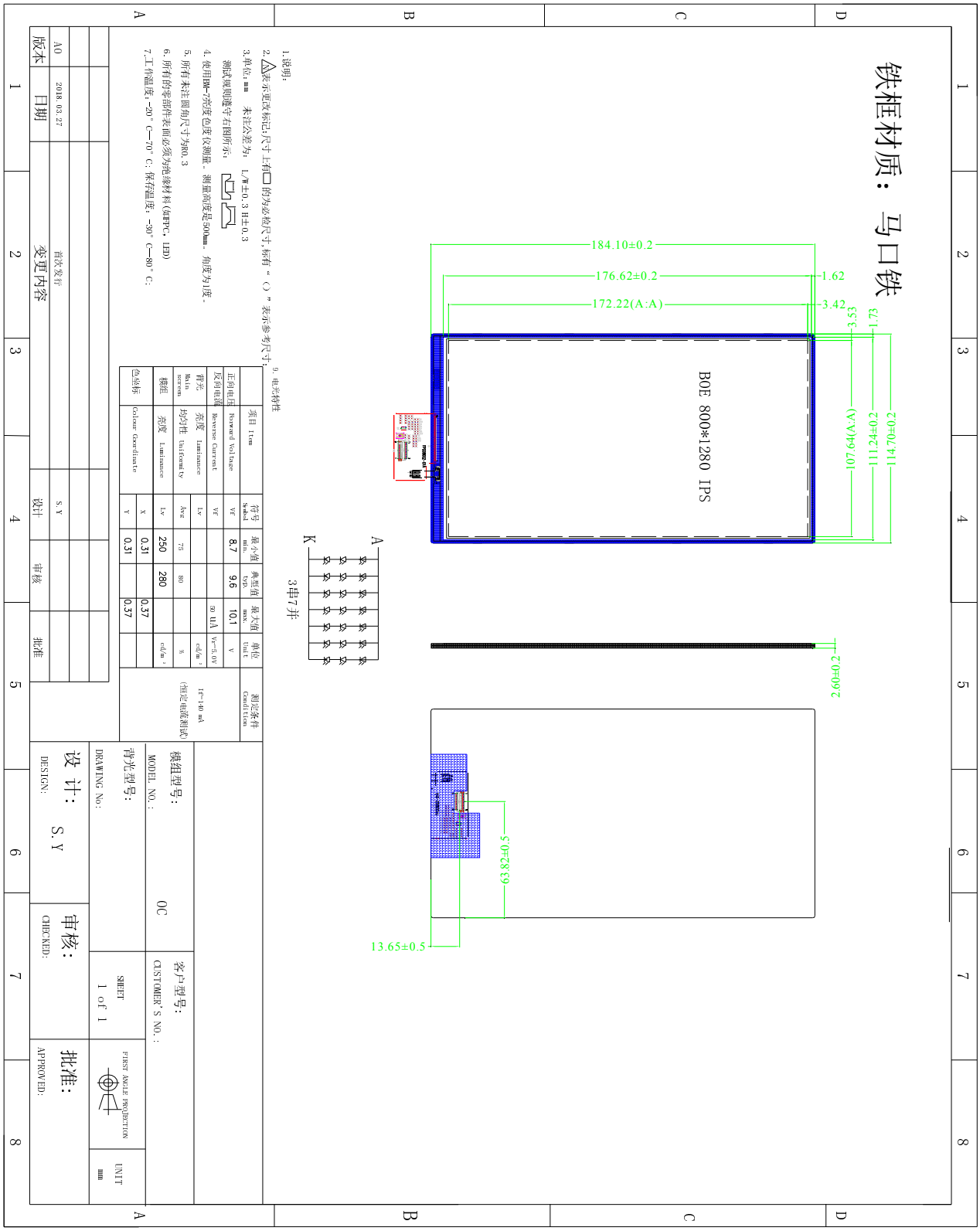
Document revision history :

DOCUMENT REVISION	DATE	DESCRIPTION	PREPARED BY	APPROVED BY
A	2018.03.25	First Release.		

General Feature:

Item	Standard Value	Unit
Display Size	8.0”	inch
Number of Pixels	800 x 3(RGB) x 1280	pixels
Active Area	107.64(H) x 172.224(V)	mm
Pixel pitch	0.04485 X 0.13455	mm
Outline Dimension	114.70(W)*184.10(H)*2.6(T)	mm
Pixel Arrangement	RGB vertical stripe	-
Display Mode	Normally Black	-
Number of color	16.7M	-
Viewing Direction	ALL	-
Surface Treatment	Anti-Glare	-
Interface	4 lane MIPI	-
Driver Condition	VCI=3.3V typ. / VDD3=1.8V typ.	V
Backlight	White LED	-
Touch Panel	No Touch Panel	-
Operation Temperature	-20 to +60	℃
Storage Temperature	-30 to +80	℃
Weight	TBD	g

Mechanical Dimension

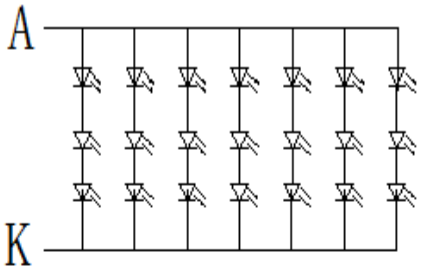


Pin Description

Interface Connector: FH26W-39S-0.3SHW(Hirose)

No.	Symbol	Function	Remark
1	LED+	LED Anode	
2	LED+	LED Anode	
3	LED+	LED Anode	
4	GND	Ground	
5	LED-	LED Cathode	
6	LED-	LED Cathode	
7	LED-	LED Cathode	
8	LED-	LED Cathode	
9	GND	Ground	
10	GND	Ground	
11	RXIN2+	MIPI data positive signal	
12	RXIN2-	MIPI data negative signal	
13	GND	Ground	
14	RXIN1+	MIPI data positive signal	
15	RXIN1-	MIPI CLK negative signal	
16	GND	Ground	
17	RXCLKIN+	MIPI CLK positive signal	
18	RXCLKIN-	MIPI data negative signal	
19	GND	Ground	
20	RXIN0+	MIPI data positive signal	
21	RXIN0-	MIPI data negative signal	
22	GND	Ground	
23	RXIN3+	MIPI data positive signal	
23	RXIN3-	MIPI data negative signal	
25	GND	Ground	
26	TE	Tearing Effect	
27	RESET	Global reset pin	
28	ID	ID PIN	
29	VDDL	Logic Supply (1.8V)	
30	VDDP	Power supply (3.3V)	
31	VDDP	Power supply (3.3V)	

LED back light specification (per a chip)



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9. 电光特性

	项目 Item	符号 Symbol	最小值 min.	典型值 typ.	最大值 max.	单位 Unit	测定条件 Condition
正向电压	Forward Voltage	Vf	8.7	9.6	10.1	V	If=140 mA (恒定电流测试)
反向电流	Reverse Current	Vf			50 uA	Vr=5.0V	
背光 Main screen	亮度 Luminance	Lv				cd/m ²	
	均匀性 Uniformity	Avg	75	80		%	
模组	亮度 Luminance	Lv	250	280		cd/m ²	
色坐标	Colour Coordinate	X	0.31		0.37		
		Y	0.31		0.37		

Electrical Characteristics

Parameter	Symbol	Value	Unit	Remarks
TFT Gate ON Voltage	VGH	12~17	V	VGH-VGL≤30V
TFT Gate OFF Voltage	VGL	-7~-16	V	
TFT Common Electrode Voltage	VCOMH	0	V	
	VCOML	-2	V	

Notes :
1. VGH is TFT Gate operating voltage.
2. VGL is TFT Gate operating voltage. The low voltage level of VGL signal must be fluctuates with same phase as Vcom.
3. Vcom must be adjusted to optimize display quality, as Crosstalk and Contrast Ratio etc..
4. The value is just the reference value. The customer can optimize the setting value by the different D-IC

Absolute maximum ratings

Parameter	Symbol	Spec.			Unit	Note
		Min.	Typ.	Max.		
I/O voltage	VDDIO_IF	1.8	-	3.6	V	
	VDDIO					
Power input	VDD	2.5	-	3.6	V	
VSP voltage	VSP	4.5	-	6	V	
VSN voltage	VSN	-4.5	-	-6	V	
VOTP power	VOTP	-	7.5	-	V	
Operating Temperature		-20	-	85	℃	(1)

Note :(1) Do not let condensation for low temperature

Table 12.1: Absolute maximum rating

Typical operating condition

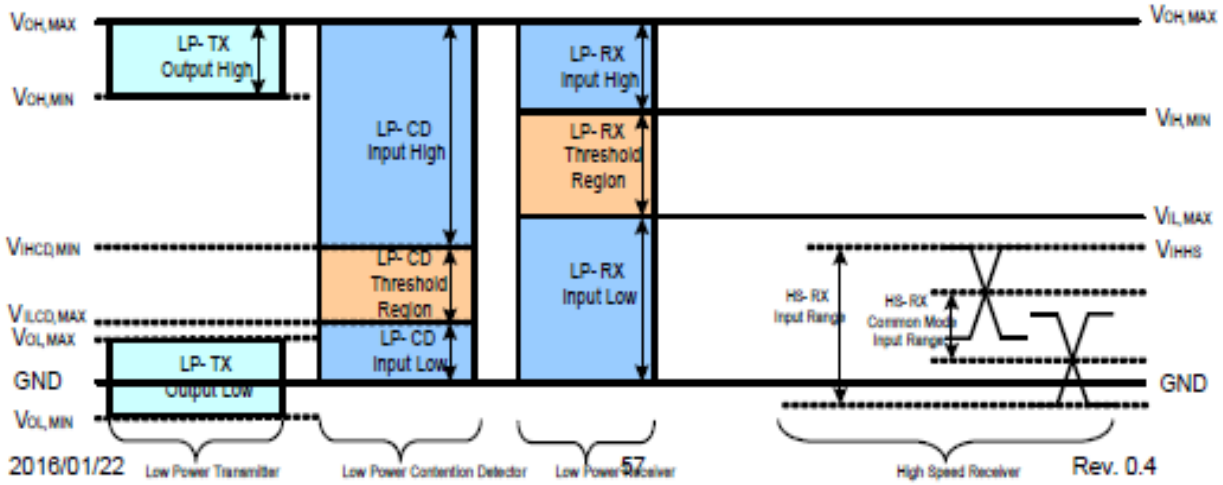
Parameter	Symbol	Spec.			Unit	Note
		Min.	Typ.	Max.		
VDD voltage	VDD	-	3.3	-	V	Digital supply voltage
VDDP voltage	VDDP	-	3.3	-	V	Analog supply voltage
VDDIO voltage	VDDIO	-	3.3	-	V	I/O Power supply voltage
VOTP voltage	VOTP	-	7.5	-	V	Programming voltage
VSP voltage	VSP	4.5	5.0	6	V	VSP voltage
VSN voltage	VSN	-4.5	-5.0	-6	V	VSN voltage
VGH voltage	VGH	9.3	-	18	V	VGH voltage
VGL voltage	VGL	-16	-	-6.7	V	VGL voltage

Table 12.2 : Typical operating conditions

DC Characteristics

(Test condition: VCI=1.6~3.6V, TA=-20℃~+85℃,VSS=VSSA=0V)

Parameter		Symbol	Spec. Min.	Typ.	Max.	Unit	Note
VDDIO Input high level voltage		VIH	0.8 x VDDIO		VDDIO	V	
VDDIO input low level voltage		VIL	VSS		0.2 x VDDIO	V	
Input Leakage Current		Ileak	(-1)		(+1)	μA	
VGL_REG2 output voltage		VGL_REG2		TBD		V	
VGMP output voltage		VGMP		TBD		V	
VGMN output voltage		VGMN		TBD		V	
VCI1 output voltage		VCI1		TBD		V	
VGL output voltage		VGL_O	-16		-6	V	
VGH output voltage		VGH_O	8		19	V	
VCL output voltage		VCL	-2.1	-2.4	-3	V	
VOM output voltage		VCOM	-2.75	-1.48	-0.2	V	
Input terminal resistance		ZID		100		ohm	
Source output level deviation	Graycode = 0 ~ 14 Graycode = 241 ~ 255			TBD		mV	
	Graycode = 15 ~ 31 Graycode = 208 ~ 240			TBD		mV	
	Graycode = 32 ~ 207			TBD		mV	
Source output offset deviation	Graycode = 0 ~ 14 Graycode = 241 ~ 255	-		TBD		mV	
	Graycode = 15 ~ 31 Graycode = 208 ~ 240	-		TBD		mV	
	Graycode = 32 ~ 207	-		TBD		mV	
Current consumption	Analog Operating	IAOP		TBD		mA	
	Analog Stand-by	IAST		TBD		mA	
Rush current		Ivddpeak		TBD		mA	
VOTP operation current		Ivpp		TBD		mA	



MIPI AC characteristics

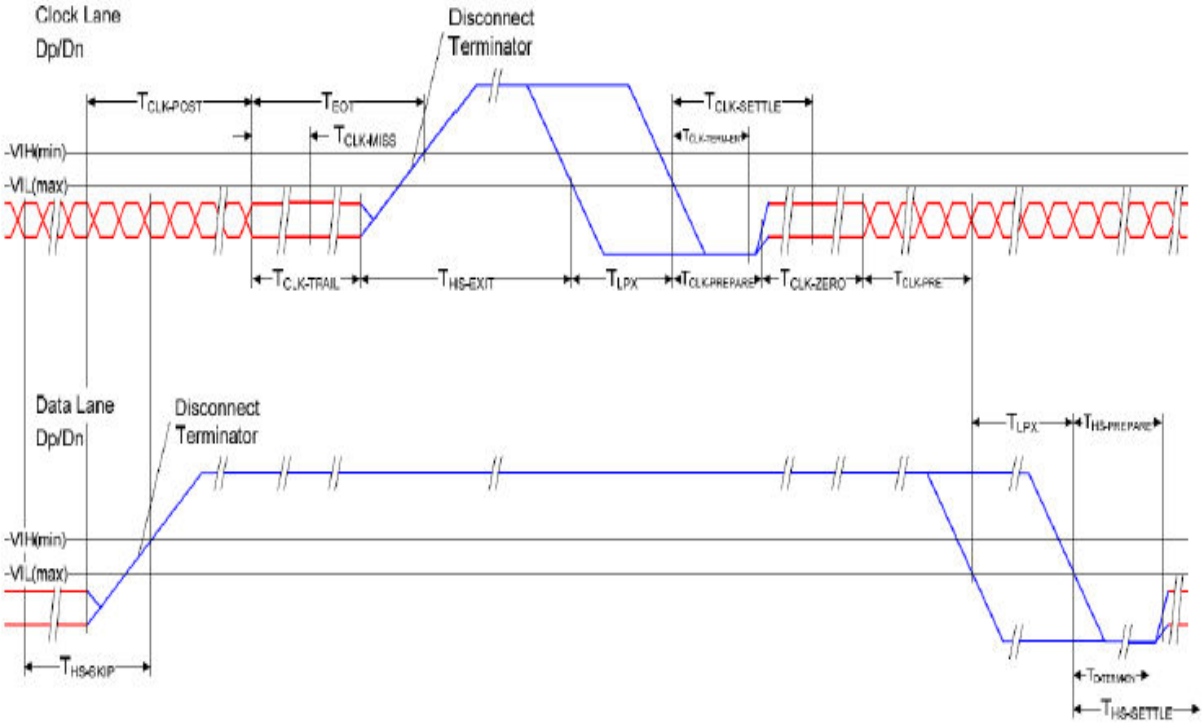


Figure 13.1: Switching the clock lane between clock transmission and low-power mode

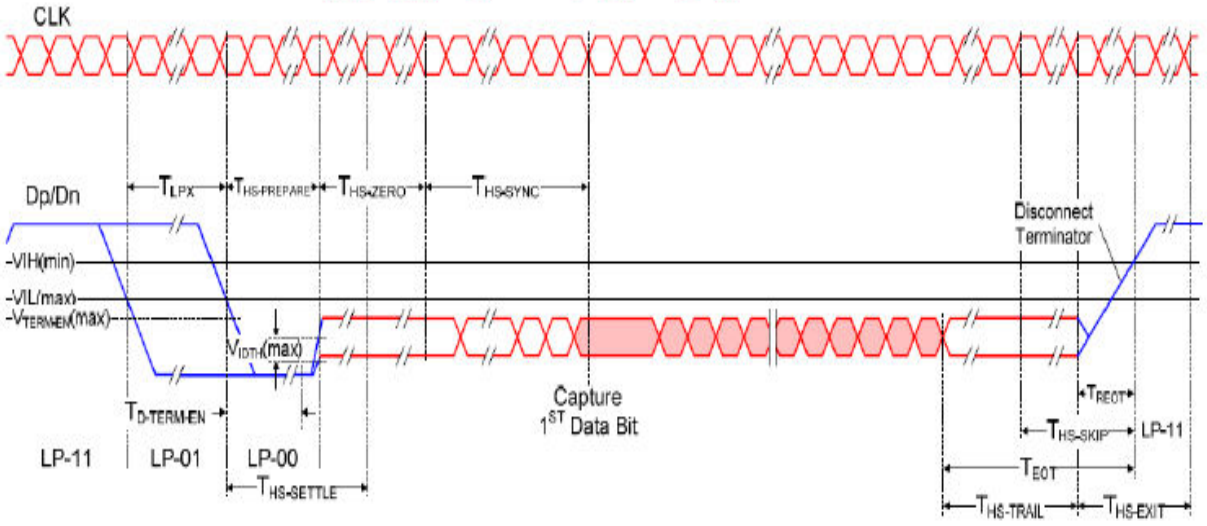


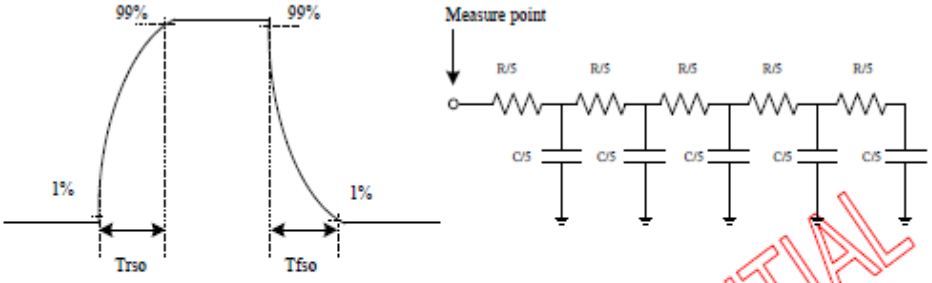
Figure 13.2: Timing of high-speed data transmission in bursts

MIPI data-clock timing specification

Parameter	Descript	Spec. Min.	Typ.	Max.	Unit
T_{REOT}	30%-85% rise time and fall time	-	-	35	ns
$T_{CLK-MISS}$	Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-RX.	-	-	60	ns
$T_{CLK-POST}$*1	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of $T_{HS-TRAIL}$ to the beginning of $T_{CLK-TRAIL}$.	60 ns + 52*UI (For DCS)	-		ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8	-		ns
$T_{CLK-SETTLE}$	Time interval during which the HS receiver shall ignore any Clock Lane HS transitions, starting from the beginning of $T_{CLK-PRE}$.	95	-	300	ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach VTERM-EN	-	38	ns
$T_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of $T_{HSPREPARE}$.	85 ns + 6*UI	-	145 ns + 10*UI	ns
T_{EOT}	Time from start of $T_{HS-TRAIL}$ or $T_{CLK-TRAIL}$ period to start of LP-11 state	-	-	105ns+48*UI	-
$T_{HS-EXIT}$ (1)	time to drive LP-11 after HS burst	100	-	-	ns
$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	40ns + 4*UI	-	85ns+6*UI	ns
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + Time to drive HS-0 before the Sync sequence	145ns + 10*UI	-	-	ns
$T_{HS-SKIP}$	Time-out at RX to ignore transition period of EoT	40	-	55ns+4*UI	ns
$T_{HS-TRAIL}$	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60 + 4*UI	-	-	ns
T_{LPX}	Length of any Low-Power state period	50	-	-	ns
Ratio T_{LPX}	Ratio of $T_{LPX(MASTER)}/T_{LPS(SLAVE)}$ between Master and Slave side	2/3	-	3/2	-
T_{TA-GET}	Time to drive LP-00 by new TX	$5*T_{LPX}$			ns
T_{TA-GO}	Time to drive LP-00 after Turnaround Request	$4*T_{LPX}$			ns
$T_{TA-SURE}$	Time-out before new TX side starts driving	T_{LPX}	-	$2*T_{LPX}$	ns

Note: (1) For image transmission:
$T_{CLK-POST}$ min value =164 when MIPI max frequency per lane = 0.53Gbps.
$T_{CLK-POST}$ min value =112 when MIPI max frequency per lane = 1Gbps

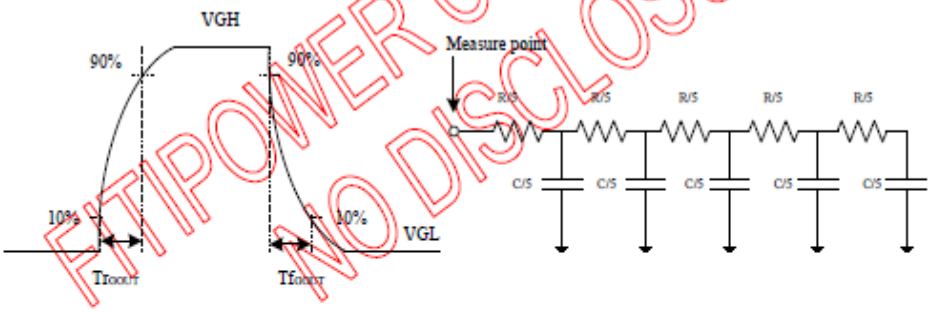
Source output timing (SOUT1 ~ SOUT2400, SDUMY[3:0])



Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max	
Source driver rising time	Trso	TBD	-	-	TBD	µs
Source driver falling time	Tfso	TBD	-	-	TBD	µs

Table 13.3: Source output timing

Panel control signal output (GOUTL[1]~GOUTL[22] , GOUTR[1]~GOUTR[22])



Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max	
Panel control signal rising time	T_{rGOUT}	TBD	-	-	TBD	µs
Panel control signal falling time	T_{fGOUT}	TBD	-	-	TBD	µs

Table 13.4: GOA output timing

Serial interface characteristics

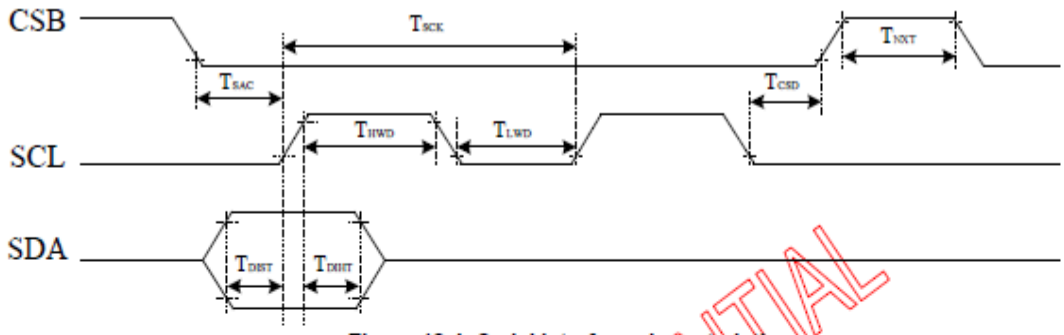


Figure 13.4: Serial interface characteristics

Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max	
CSB assertion to first clock edge	T_{SAC}		120	-	-	ns
CSB deassertion frome last clock edge	T_{CSD}		120	-	-	ns
CSB next control enable	T_E		200	-	-	ns
SCL period time	T_{SCK}		200	-	-	ns
SCL high period time	T_{HWD}		100	-	-	ns
SCL low period time	T_{LWD}		100	-	-	ns
SDA input data setup time	T_{DIST}		50	-	-	ns
SDA input data hold time	T_{DIHT}		50	-	-	ns

Timing requirements for RESETB

When RESETB of the reset pin equals to Low, it will be in the condition of reset. When it is in the condition of reset, it will make the device recover the initial set.

However, in order to avoid the reset noise cause reset, there is a mechanism to judge about whether the reset is needed or not.

The closed interval of Low can be shown as the following.

(Test condition: VDDIO=1.65V~3.6V, VSS=0V, T_A=-20 ~+85)

Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max	
Reset low pulse width	Trst		20	-	-	µs

Figure 13.5: Reset timing

Power On/Off Sequence

Power on sequence PMODE[1:0]=01b

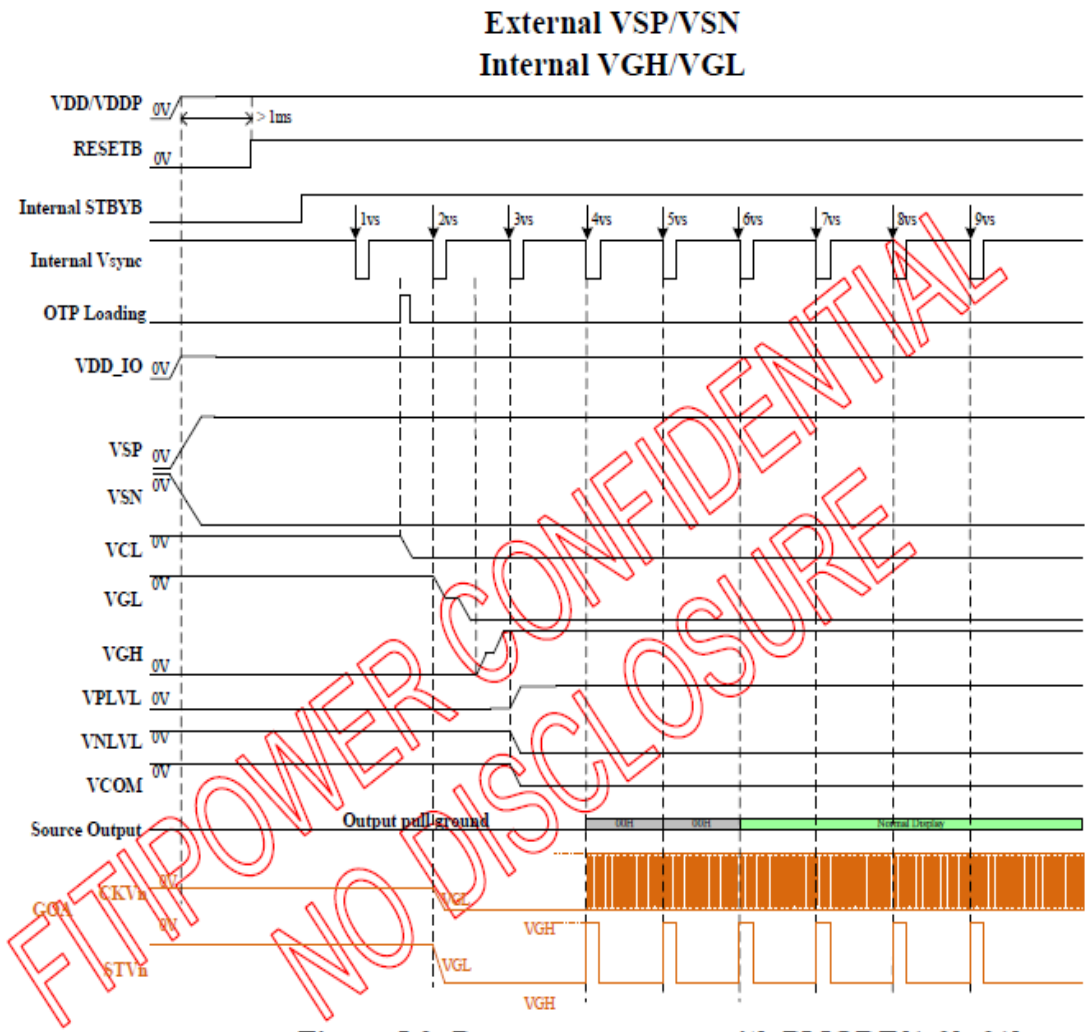


Figure 5.3: Power on sequence with PMODE[1:0]=01b

Power off sequence PMODE[1:0]=01b

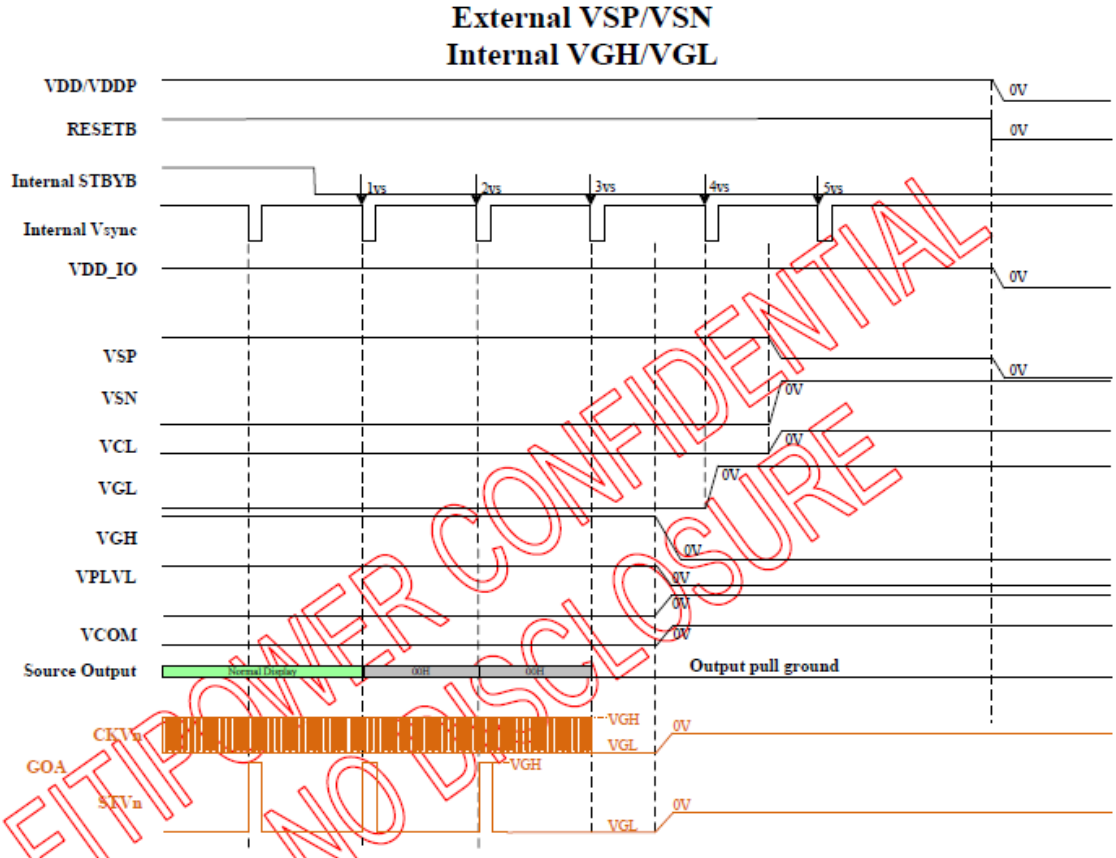


Figure 5.4: Power off sequence with PMODE[1:0]=01b

LVDS/MIPI Input Timing Table

For 800RGBx1280

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
MIPI (4 Lane) @Frame rate=60Hz			432		Mbps
MIPI (3 Lane) @Frame rate=60Hz			576		Mbps
DCLK frequency @Frame rate=60Hz	F_{DCLK}		71.9		MHz
HSYNC period time	T_H		920		DCLK
Horizontal display area	T_{HD}		800		DCLK
HSYNC pulse width	T_{HPW}		24	-	DCLK
HSYNC back porch	T_{HBP}		24	-	DCLK
HSYNC front porch	T_{FBP}		72	-	DCLK
VSYNC period time	T_V		1304		H
Vertical display area	T_{VD}		1280		H
VSYNC pulse width	T_{VPW}		2	-	H
VSYNC back porch	T_{VBP}		10	-	H
VSYNC front porch	T_{VFP}		12	-	H

MIPI Frequency = (Frame rate) x TH x TV x 24bits.

RECOMMEND VALUE OF WIRING RESISTANCE AND CAPACITORS

Recommended specification of wiring resistance and capacitors

Pad Name	Pin Definition	Maximum series resistance(ohm)
VDDIO,VDDIO_IF	Power supply	5
VDD,VDDP	Power supply	5
VSS,VSSA,VSS_IF,VSSP	Power supply	5
VOTP	OTP Power supply	10
RESETB,CSB,SCL,SDA,SCL_I2C,SDA_I2C	Input	100
PMODE[1:0],LANE1_STBYB,LANE0_BISTB,LNSW[1:0],RES[2:0],PNSW	Input	100
VCSW1,VCSW2,LEDPWM,LEDON,ERR_FG	Output	100
DP[0],DN[0]	Input+Output	5
DP[1],DN[1],DP[2],DN[2],DP[3],DN[3],CKP,CKN	Input	5
VCOM	Output,Capacitor connection	5
VDD_18V,VDD_18V_IF	Output,Capacitor connection	5
VSP,VSN,VCL	Output,Capacitor connection	10
VGMP,VGMN,VREF	Output,Capacitor connection	10
VGH,VGH_REG,VGL,VGL_REG	Output,Capacitor connection	10
C41P,C41N,C42P,C42N,C51P,C51N,C11P_VGL,C11N_VGL	Capacitor connection	5
GOUTL[22:1],GOUTR[22:1]	Output	50

Pad Name	Withstanding voltage (V)	CAP (uF)
VGH	25	1
VGL	25	1
VGH_REG	25	1
VGL_REG	25	1
VSP	10	1
VSN	10	1
VGMP	10	1
VGMN	10	1
VCOM	6.3	2.2
VDD/VDDP	6.3	2.2
VDDIO/VDDIO_IF	6.3	2.2
VDD_18V	6.3	1
VDD_18V_IF	6.3	1
VCL	6.3	1
VCI1	6.3	1
C41P/C41N	25	1
C42P/C42N	25	1
C51P/C51N	25	1

Optical Characteristics

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing Angle range	Horizontal	Θ_3	CR > 10	80	89	-	Deg.	WV-Pol Note 1
		Θ_9		80	89	-	Deg.	
	Vertical	Θ_{12}		80	89	-	Deg.	
		Θ_6		80	89	-	Deg.	
Luminance Contrast ratio		CR	Θ = 0°	700	800	-		-
Cell Transmittance		Tr		-	4.6%	-	%	
White Chromaticity		x_w		-	0.301	-		Note 4 CF Glass
		y_w		-	0.328	-		
Reproduction of color (C light)	Red	R_x		-	0.628	-		
		R_y		-	0.331	-		
	Green	G_x		-	0.279	-		
		G_y		-	0.551	-		
	Blue	B_x		-	0.140	-		
		B_y		-	0.142	-		
Color Gamut (C light)				-	55	-	%	NTSC
Response Time (Rising + Falling)		T_{RT}	Ta= 25° C Θ = 0°	-	30	40	ms	Note 5

RELIABILITY TEST

Test Item	Test Condition	Remark
High Temperature Storage	*Ta=70℃; 96hrs*	*IEC60068-2-1：2007 GB2423.2-2008*
Low Temperature Storage	*Ta=-20℃; 96hrs*	*IEC60068-2-1：2007 GB2423.1-2008*
High Temperature Operation	*Ta=60℃; 96hrs*	*IEC60068-2-1：2007 GB2423.2-2008*
Low Temperature Operation	*Ta=-10℃; 96hrs*	*IEC60068-2-1：2007 GB2423.1-2008*
High Temperature High Humidity Operation	*Ta=50℃ 80%RH；96hrs(no condensation)*	*IEC60068-2-78：2001 GB/T2423.3-2006*
Thermal Shock	*-20℃(0.5h) ~ 70℃(0.5h) / 10 cycles*	*Start with cold temperature; End with high temperature; IEC60068-2-14:1984,GB2423.22-2002*
Image Sticking	*25℃; 4hrs*	*Note1*
ElectrostaticDischarge	*Contact=±4KV,classB Air=±8KV,classB*	

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